Amendments to the specification:

Please replace the paragraph beginning on page 103, line 20, with the following rewritten paragraph:

D1

-- Six of the amplifiers in the amplifier portion 222 may be connected in parallel between the output of the tri-region voltage circuit 224 and the bus 266 which carries the peripheral voltage Vcc and twelve of the amplifiers in the amplifier portion 222 may be connected in parallel between the output of the tri-region voltage circuit 224 and the bus 267 which carries the array voltage Vcca. The power buses 266 and 267 are isolated except for a twenty ohm resistor 269 that bridges the two buses together. Isolating the buses is important because it keeps high current spikes that occur in the array from ~~effecting~~ affecting the peripheral circuits. Failure to isolate buses 266 and 267 can result in speed degradation for the DRAM because large current spikes in the array may cause voltage cratoring and a corresponding slowdown in logic transitions. With isolation, the peripheral voltage Vcc is almost immune to array noise. --

Please replace the paragraph beginning on page 108, line 16, with the following rewritten paragraph:

D2

-- More specifically, in the preferred embodiment, the power amps 260 are configured with a certain load capacitance and compensation network such that their slew rate and voltage stability are considered optimum when there is about 0.25 nanofarads of decoupling capacitance in the array block per power amplifier. In the disclosed embodiment, a group of twelve power amplifiers (277 in FIG. 35), includes eight that are respectively associated with each one of the eight array blocks and four additional amplifiers that are not affected by the array switches. When a switch is opened that disables an array block and its associates decoupling capacitors, a signal is input to the control circuit 226 to disable the corresponding power amplifier to maintain the correct, optimal, relationship. In ~~additional~~ addition to maintaining voltage stability, that reduces unneeded current consumption. In general, more

cont D2

decoupling capacitance is better for voltage stability and lower ripple but is worse for amplifier slew rate and hence an optimum is sought to be maintained. - -

Please replace the paragraph beginning on page 112, line 23, with the following rewritten paragraph:

- - A second portion 312 of the circuit 308 produces the signal VBBOK* which is directly input to the oscillator 300. The signal VBBOK* speeds up the oscillator. The first circuit portion 310 and the second circuit portion 312 are the same circuit, and both operate as differential amplifiers. Basically, regardless of the specific circuit design, the Vbb differential regulator 2 circuit 308 should be constructed using low-biased current sources and pMOS diodes to translate the pump voltage Vbb to a normal voltage level. The reader seeking additional information concerning the Vbb differential regulator 2 circuit 308 is directed to U.S. Patent Application Serial No. 08/668,347 entitled Differential Voltage Regulator, filed 6/26/1996, and assigned to the same assignee as the present invention ~~(Micron No. 96-172)~~. - -

D3

Please replace the paragraph beginning on page 118, line 16, with the following rewritten paragraph:

- - FIG. 40H illustrates the details of the oscillator 424. The oscillator 424 is a ring-type oscillator similar to the oscillator 300 illustrated in FIG. 38B. The oscillator 424 has a variable a frequency so that, for example, the pump circuits 410-415 may be operated at a higher frequency during powerup to more quickly bring the Vccp bus to its operating voltage. The oscillator 424 includes a series of inverters 478 which loops back on itself to form a ring. The time required for a signal to propagate through the inverters 478 determines the period of the signal OSC. Multiple frequency operation is implemented by the inclusion of several multiplexers 479 which receive signals from various tap points in the chain of inverters 478. The multiplexers are controlled by a signal VPWRUP* and produce a higher frequency OSC signal by reducing the number of inverters 478 in the ring. - -

D4

Please replace the paragraph beginning on page 119, line 17, with the following rewritten paragraph:

-- FIG. 40J illustrates the details of the differential regulator circuit 428 shown in FIG. 39. The differential regulator circuit 428 generates an enable signal DIFFVCCPON by comparing Vccp with a reference voltage in a differential amplifier 486. When Vccp is below the reference voltage, a high value of the enable signal is generated to enable the oscillator 424. When Vcc is above the reference voltage, a low value of the enable signal is generated to disable the oscillator 424. A similar differential regulator circuit is disclosed in U.S. Patent Application S.N. 08/521,563 entitled Improved Voltage Regulator Circuit, filed 6/30/1995, and assigned to the same assignee as the present invention ~~(Micron No. 94-088)~~. --

Please replace the paragraph beginning on page 128, line 10, with the following rewritten paragraph:

-- Similarly, a resistor 606, current source 585, and current sink 590 form a negative current differential circuit for determining whether the present pullup current is less than the past pullup current. When the sink current through transistor 590 is greater than the source current through transistor 585, the additional sink current flows from Vcc through resistor 606 and into transistor 590. As a result, a voltage at an input terminal of an inverter 608 is lowered. When the voltage at the input terminal of the inverter 608 becomes a low logic value, the signal PULLUPOK2 will change to a low logic value as a result of the series connection of inverter 608 with an inverter 609 thereby indicating that the pullup current has decreased. However, when the sink current through transistor 590 is equal to or less than the source current through transistor 585, additional current builds up at the input terminal of inverter 608, causing the voltage at the input terminal of ~~inventor~~ inverter 608 to remain at a high logic value, thereby maintaining a high logic value for the PULLUPOK2 signal. --

Please replace the paragraph beginning on page 129, line 3, with the following rewritten paragraph:

-- The pullup current monitor 518 also includes the overcurrent monitor 522. The overcurrent monitor 522 includes current source 584 and generates a signal DVC2HIC indicative of whether the pullup current is excessive. The source current from transistor 584 flows into a resistor 514. ~~Resister~~ Resistor 514 converts the current into a voltage that is monitored by an inverter 616. As long as the source current is not too high, the input terminal of inverter 616 remains at a low logic state. If, however, the source current becomes excessive, the input terminal of inverter 616 changes to a high logic state and causes signal DVC2HIC to assume a high logic state, as a result of the series connection of the inverter 616 with an inverter 617, indicating an overcurrent situation. The amount of current required to trigger the overcurrent monitor is defined by the input voltage at which the inverter 616 changes states divided by the resistance of resistor 514. --

Please replace the paragraph beginning on page 131, line 2, with the following rewritten paragraph:

-- The center logic 23 illustrated in FIG. 2 is illustrated in block diagram ~~from~~ form in FIG. 43. The center logic is responsible for performing a number of functions including processing of the row address strobe signals in a RAS chain circuit 650, processing of column address strobe signals in control logic 651, row address predecoding in row address block 652, and column address predecoding in block 654. The center logic 23 also contains test mode logic 656, option logic 658, a "spares" circuit 660, and a misc. signal input circuit 662. The control portion 401 of the Vccp pump 400 (see FIG. 39) and the voltage regulator 220 (see FIG. 35) are located in the center logic. Completing the description of the center logic 23 illustrated in FIG. 43, a power up sequence circuit 1348 of the type illustrated in FIG. 100 is also provided. Each of the blocks 650, 651, 652, 654, 656, 658, 660 and 662 illustrated in FIG. 43 will now be described. The voltage regulator 220 and the control portion 401 of the

Cont D8

Vccp pump 400 have already been described hereinabove in Section VII; the power up sequence circuit 1348 is described hereinbelow in Section XI. - -